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REMARKS

The indication of allowable subject matter in claims 1-4, 6, 7, 9, 14 and 15 is acknowledged and appreciated. In view of the following remarks, it is respectfully submitted that all claims are in condition for allowance.

Claims 5 and 16 are the sole rejected independent claims and stand rejected under 35 U.S.C. § 102 as being anticipated by JP '070. This rejection is respectfully traversed for the following reasons.

Claim 5 recites in pertinent part, "a **LOW level** voltage applied to a gate of said read transistor of each pixel is set to voltage lower than a **LOW level** voltage applied to a gate of said reset transistor thereof" (emphasis added). According to one aspect of the present invention as described on page 11, lines 7-13 of Applicants' specification (one exemplary embodiment illustrated in Figures 5A-G of Applicants' drawings), a LOW level voltage applied to the gate of the exemplary read transistor 2 of the first pixel can be set to voltage lower than the LOW level voltage applied to the gate of the exemplary reset transistor 3 of the first pixel, so that the exemplary detect transistor 4 can be kept in an OFF state under conditions other than that of FIG. 5C. In one exemplary embodiment, when a low-level voltage (V2) is applied to the gate of the exemplary read transistor 2 and a low-level voltage (V3) is applied to the gate of the exemplary reset transistor 3, the read and reset transistors can be turned off in accordance with the applied low-level voltage. The corresponding low-level voltages (e.g., for turning off the respective transistors) can be set such that V2 is lower than V3. JP '070 fails to disclose or suggest corresponding low-level voltages at the gates of the alleged read 117a and reset 116a transistors being set in the manner set forth in claim 5.

Claim 16 recites in pertinent part, "wherein said single drain layer is formed above lines for connecting said storage regions to the gates of said detect transistors in said plurality of amplifying unit pixels and above signal lines for connecting to said detect transistors of said plurality of amplifying unit pixels." Support for this feature of claim 16 can be found, for example, on page 19, lines 6-10 of Applicants' specification. The alleged single drain layer 2 or 112 of JP '070 is not disclosed as being arranged in the manner specified in claim 16. Indeed, JP '070 appears to be silent as to the relative positioning of the disclosed wires/layers.

As anticipation under 35 U.S.C. § 102 requires that each and every element of the claim be disclosed, either expressly or inherently (noting that "inherency may not be established by probabilities or possibilities", *Scaltech Inc. v. Retec/Tetra*, 178 F.3d 1378 (Fed. Cir. 1999)), in a single prior art reference, *Akzo N.V. v. U.S. Int'l Trade Commission*, 808 F.2d 1471 (Fed. Cir. 1986), based on the forgoing, it is submitted that JP '070 does not anticipate claims 5 and 16, nor any claim dependent thereon. The Examiner is directed to MPEP § 2143.03 under the section entitled "All Claim Limitations Must Be Taught or Suggested", which sets forth the applicable standard for establishing obviousness under § 103:

> To establish *prima facie* obviousness of a claimed invention, all the claim limitations must be taught or suggested by the prior art. (citing *In re Royka*, 180 USPQ 580 (CCPA 1974)).

In the instant case, the pending rejection does not "establish *prima facie* obviousness of [the] claimed invention" as recited in the pending claims because the proposed combination fails the "all the claim limitations" standard required under § 103 (Gowda is not relied upon and does not appear to obviate the aforementioned deficiencies of JP '070).

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Under Federal Circuit guidelines, a dependent claim is nonobvious if the independent claim upon which it depends is allowable because all the limitations of the independent claim are contained in the dependent claims, *Hartness International Inc. v. Simplimatic Engineering Co.*, 819 F.2d at 1100, 1108 (Fed. Cir. 1987). Accordingly, as claims 5 and 16 are patentable for the reasons set forth above, it is respectfully submitted that all claims dependent thereon are also patentable. In addition, it is respectfully submitted that the dependent claims are patentable based on their own merits by adding novel and non-obvious features to the combination. Support for new claims 17-19 can be found, for example, on page 8, lines 21-22, page 19, lines 10-13 and page 19, lines 13-14 of Applicants' specification, respectively. Based on the foregoing, it is respectfully submitted that all pending claims are patentable over the cited prior art. Accordingly, it is respectfully requested that the rejections under 35 U.S.C. § 102/103 be withdrawn.

CONCLUSION

Having fully responded to all matters raised in the Office Action, Applicants submit that all claims are in condition for allowance, an indication for which is respectfully solicited. If there are any outstanding issues that might be resolved by an interview or an Examiner's amendment, the Examiner is requested to call Applicants' attorney at the telephone number shown below.

To the extent necessary, a petition for an extension of time under 37 C.F.R. 1.136 is hereby made. Please charge any shortage in fees due in connection with the filing of this paper, including extension of time fees, to Deposit Account 500417 and please credit any excess fees to such deposit account.

Respectfully submitted,
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